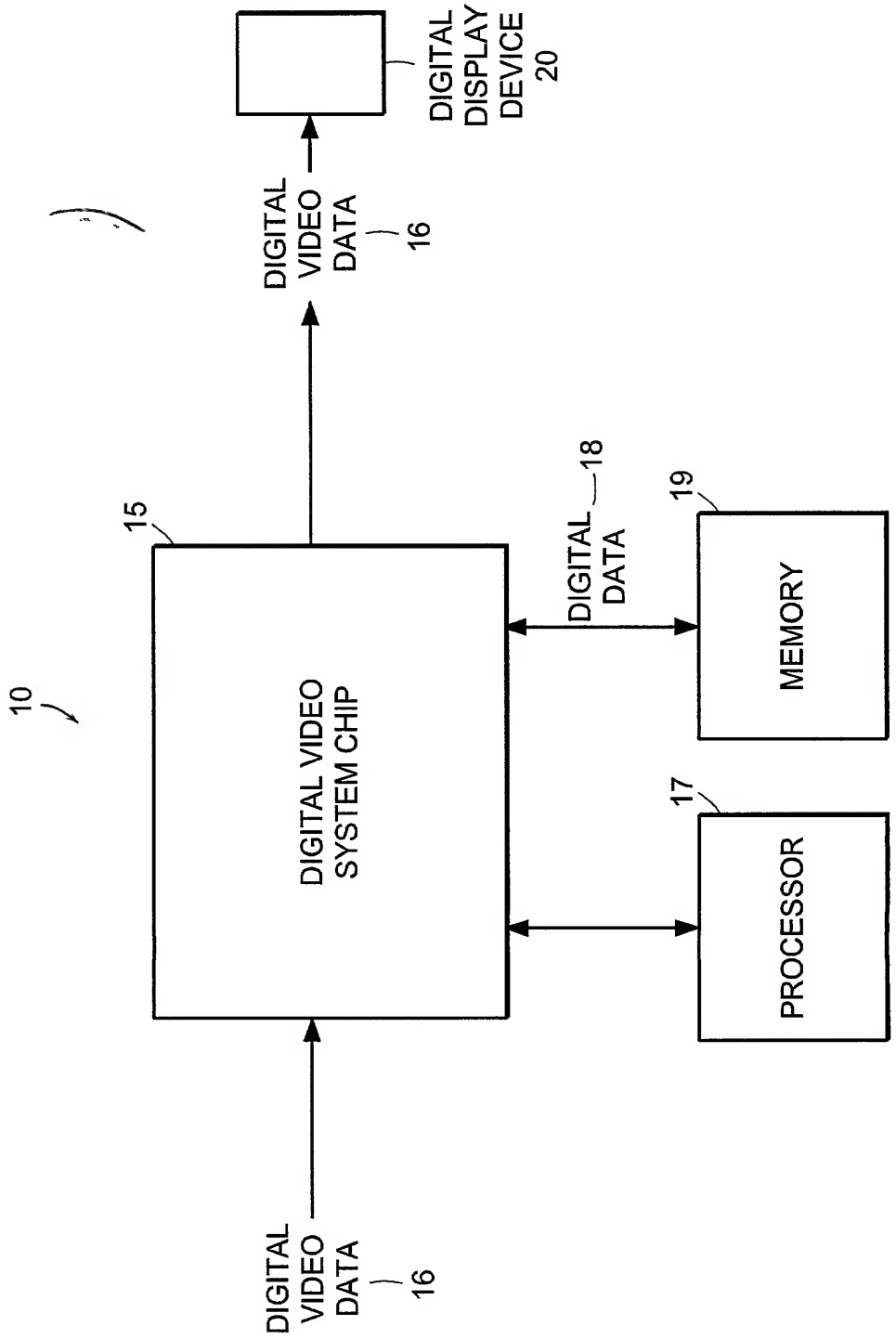

FIG. 1

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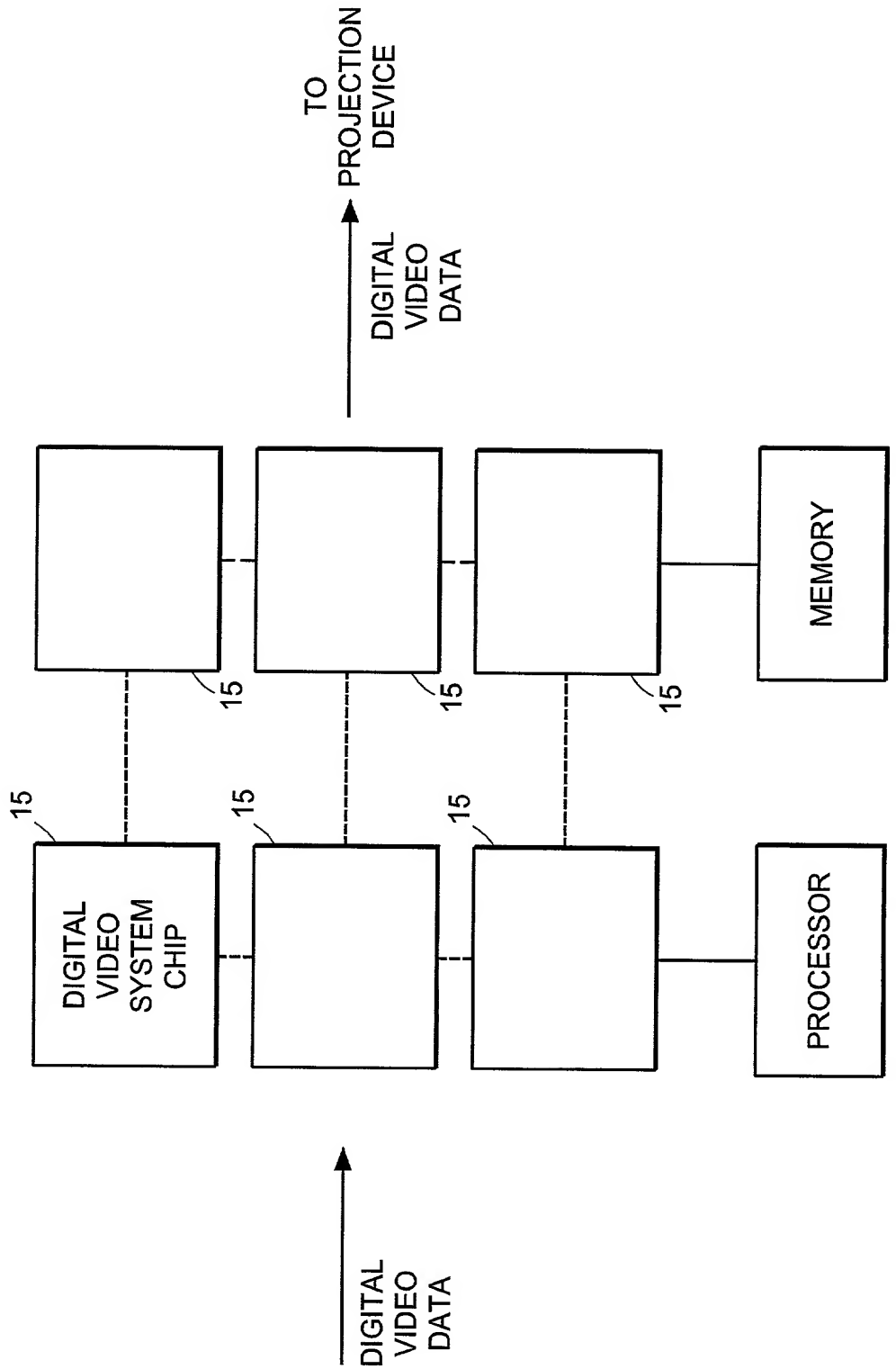
TO PROJECTION DEVICE
DIGITAL VIDEO DATA
MEMORY
15
15
15
15
15
15
DIGITAL VIDEO SYSTEM CHIP
PROCESSOR
DIGITAL VIDEO DATA

FIG. 2

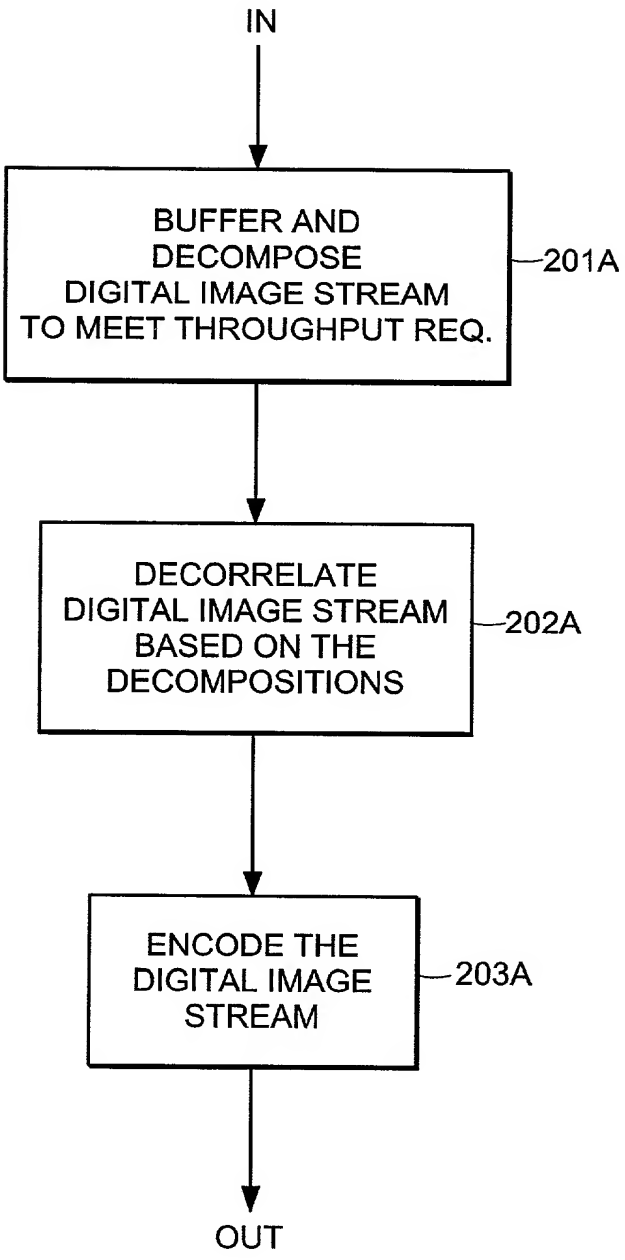

FIG. 2A

EXPRESS MAIL

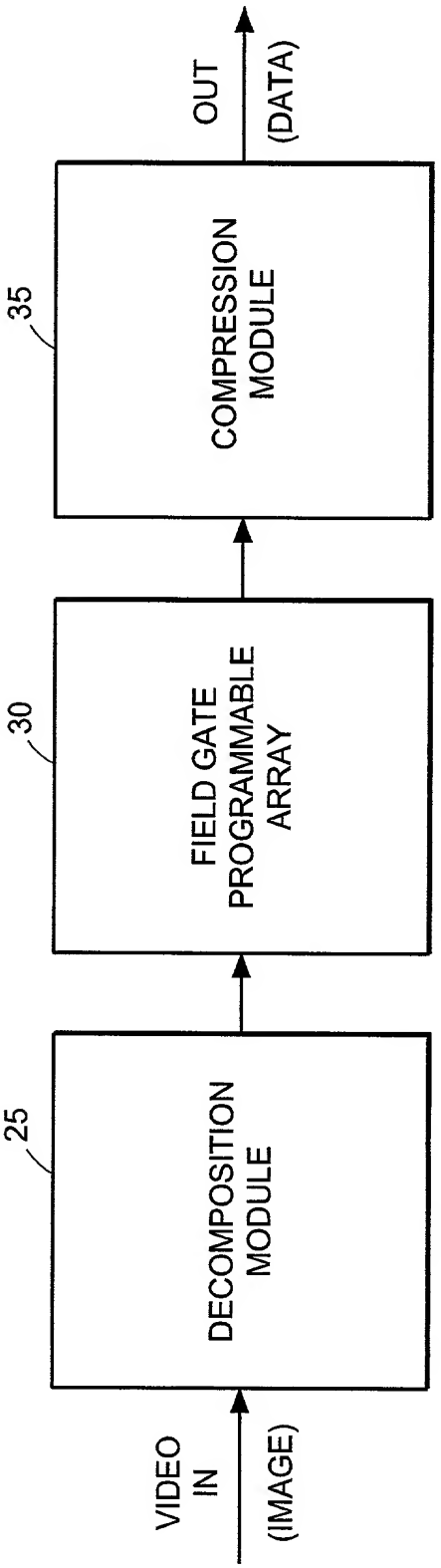
VIDEO IN
(IMAGE)
25
DECOMPOSITION MODULE
30
FIELD GATE PROGRAMMABLE ARRAY
35
COMPRESSION MODULE
OUT
(DATA)

FIG. 2B

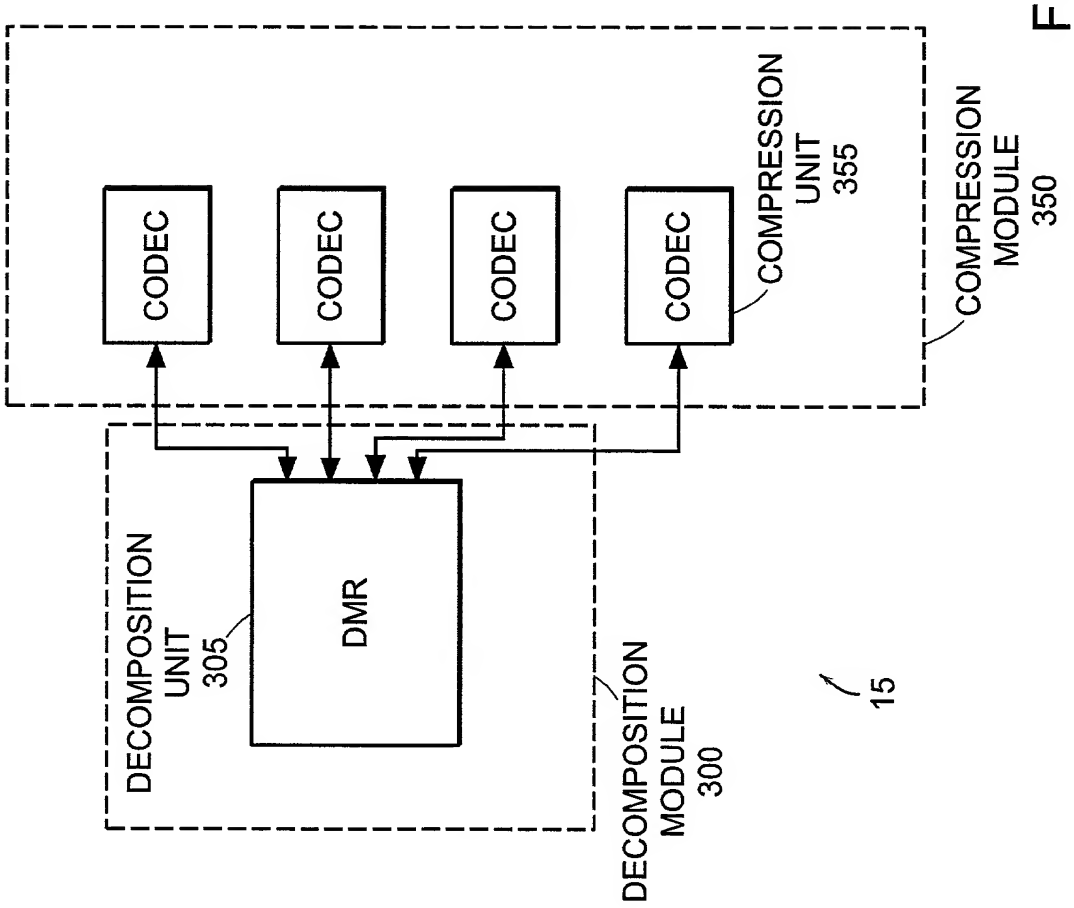
CODEC
CODEC
CODEC
CODEC
COMPRESSION UNIT 355
COMPRESSION MODULE 350
DECOMPOSITION UNIT 305
DMR
DECOMPOSITION MODULE 300
15

FIG. 3

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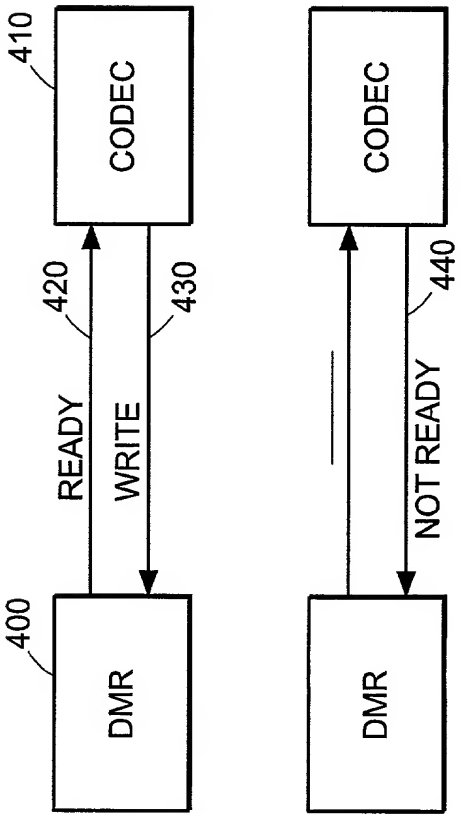

FIG. 4

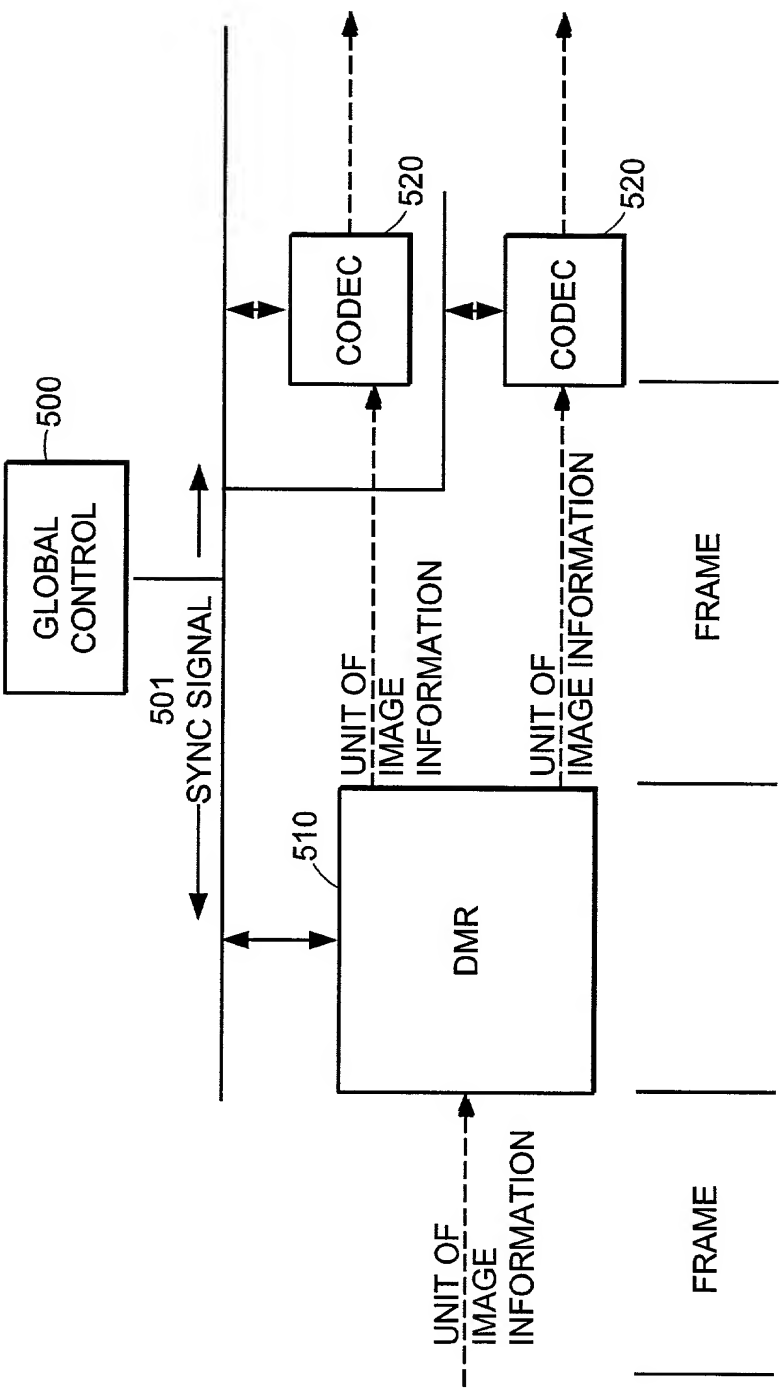
500
GLOBAL CONTROL
501
SYNC SIGNAL
510
DMR
520
CODEC
520
CODEC
UNIT OF IMAGE INFORMATION
UNIT OF IMAGE INFORMATION
UNIT OF IMAGE INFORMATION
FRAME
FRAME

FIG. 5

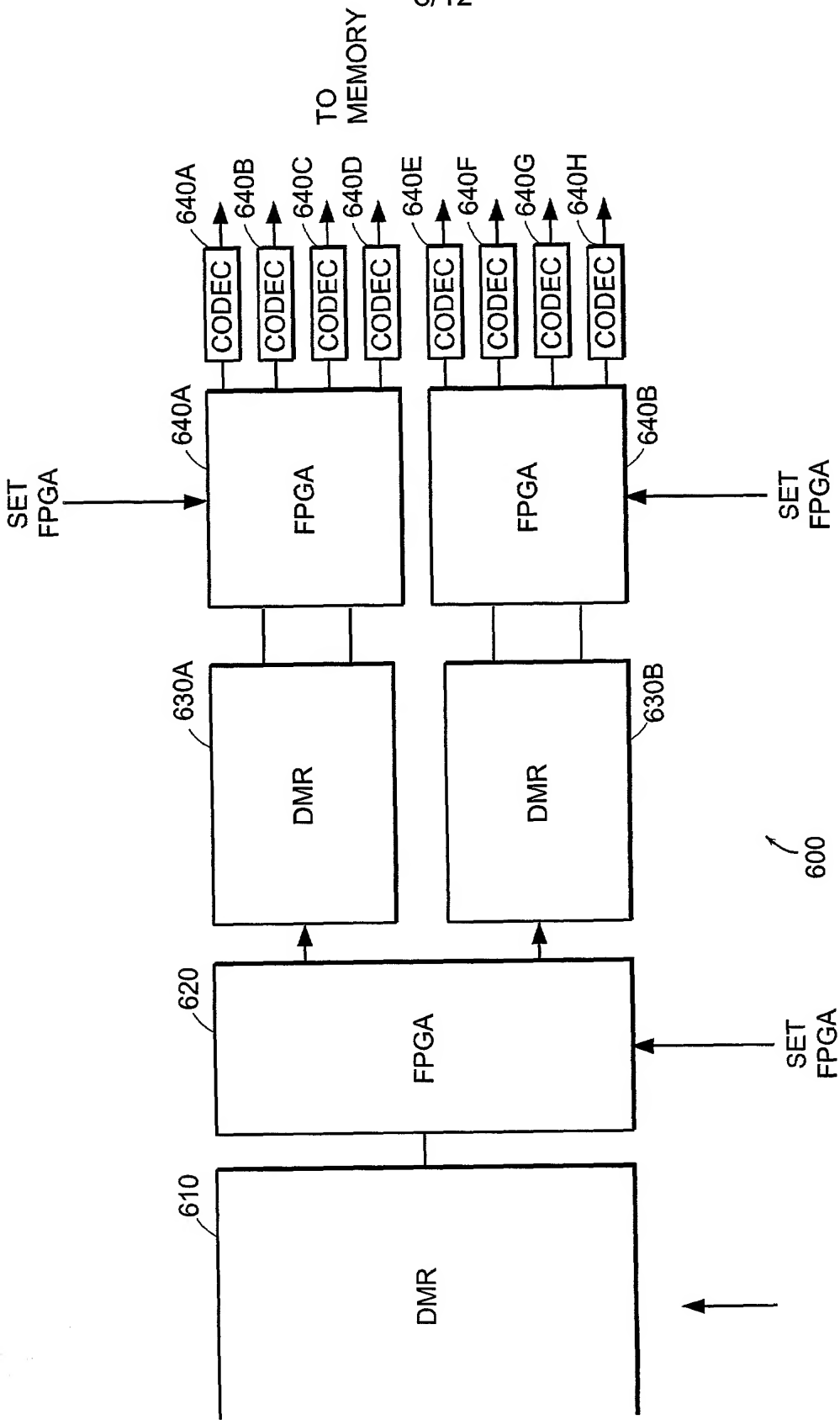
TO MEMORY
640A
640B
640C
640D
640E
640F
640G
640H
CODEC
640A
640B
FPGA
SET FPGA
630A
630B
DMR
620
610
600

FIG. 6

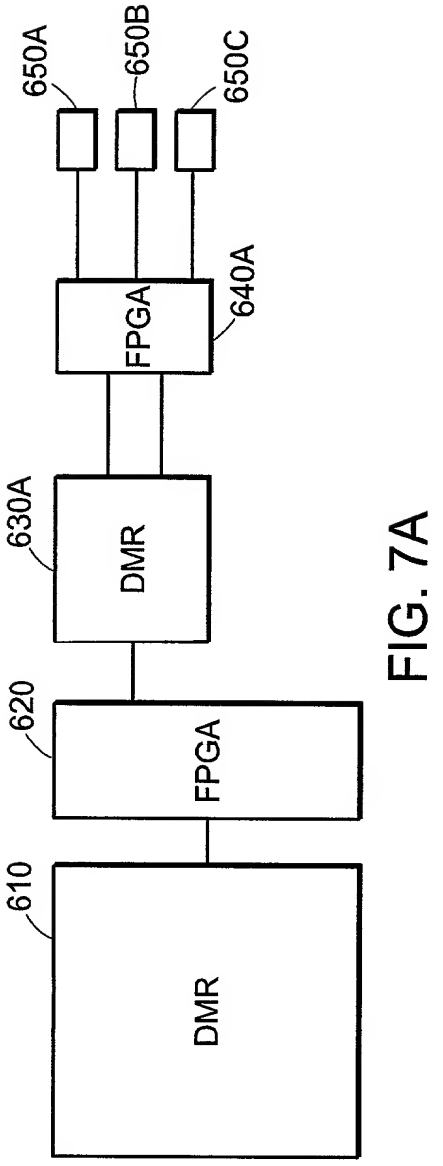
650A
650B
650C
FPGA
640A
630A
DMR
620
FPGA
610
DMR

FIG. 7A

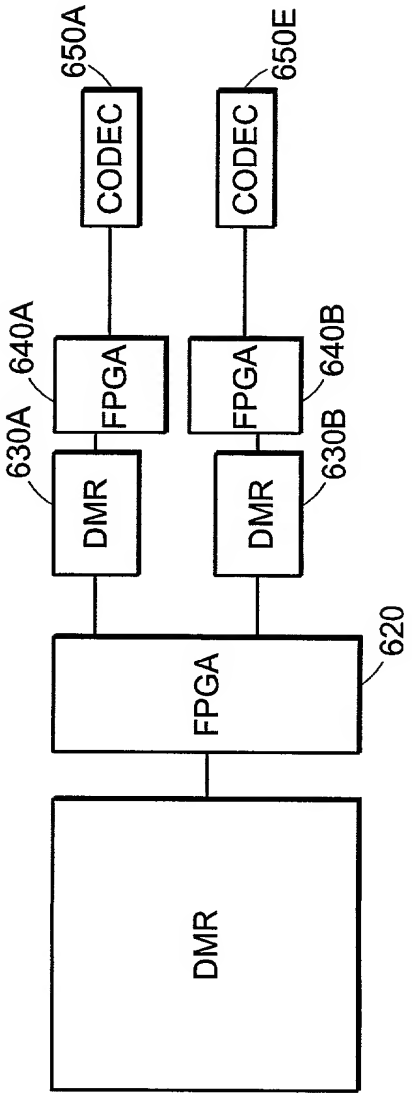
650A
650E
CODEC
CODEC
640A
FPGA
FPGA
640B
630A
630B
DMR
DMR
620
FPGA
DMR

FIG. 7B

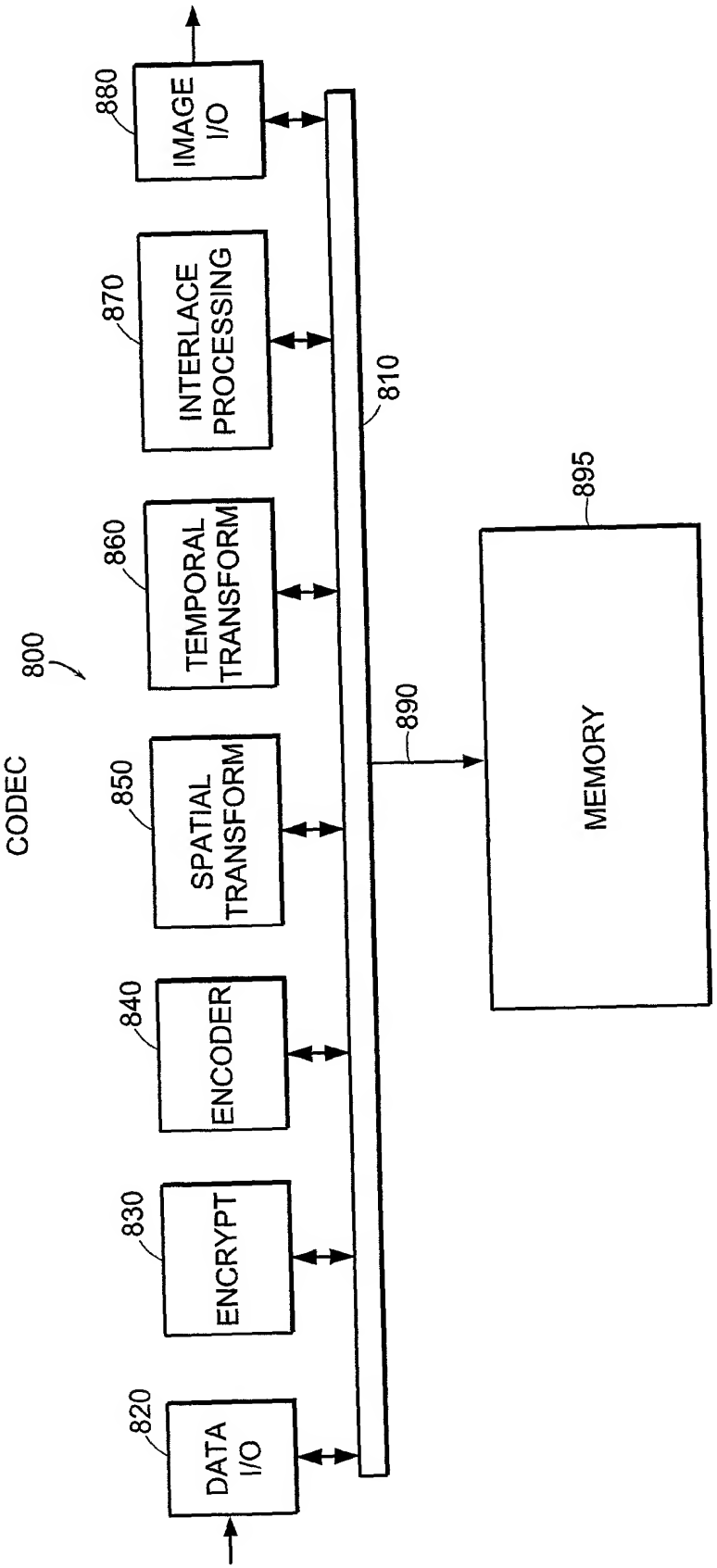

FIG. 8

20:54:30 5-23-2004

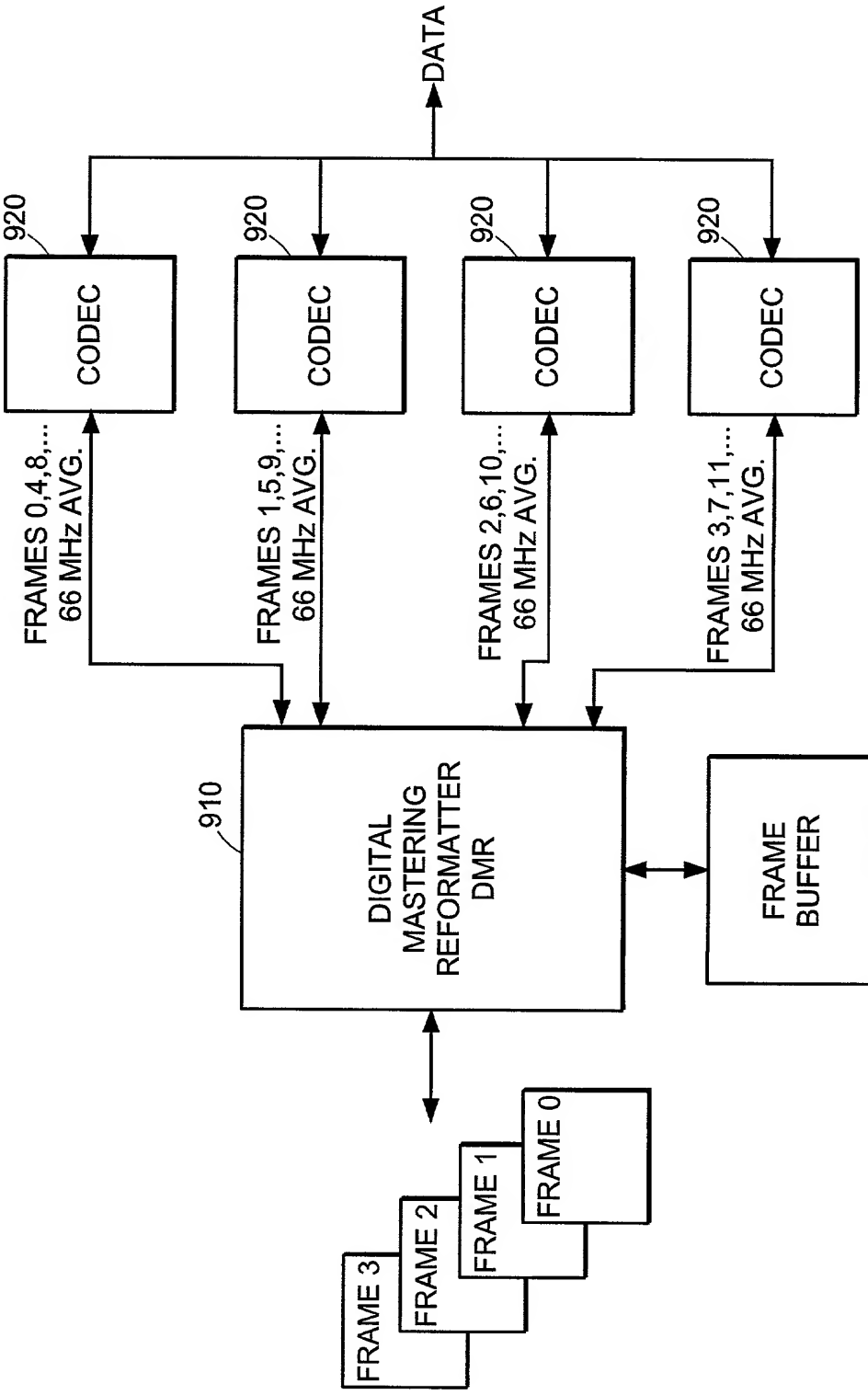
DATA
920
CODEC
920
CODEC
920
CODEC
920
CODEC
FRAMES 0,4,8,...
66 MHz AVG.
FRAMES 1,5,9,...
66 MHz AVG.
FRAMES 2,6,10,...
66 MHz AVG.
FRAMES 3,7,11,...
66 MHz AVG.
910
DIGITAL MASTERING REFORMATTER DMR
FRAME BUFFER
FRAME 0
FRAME 1
FRAME 2
FRAME 3

FIG. 9

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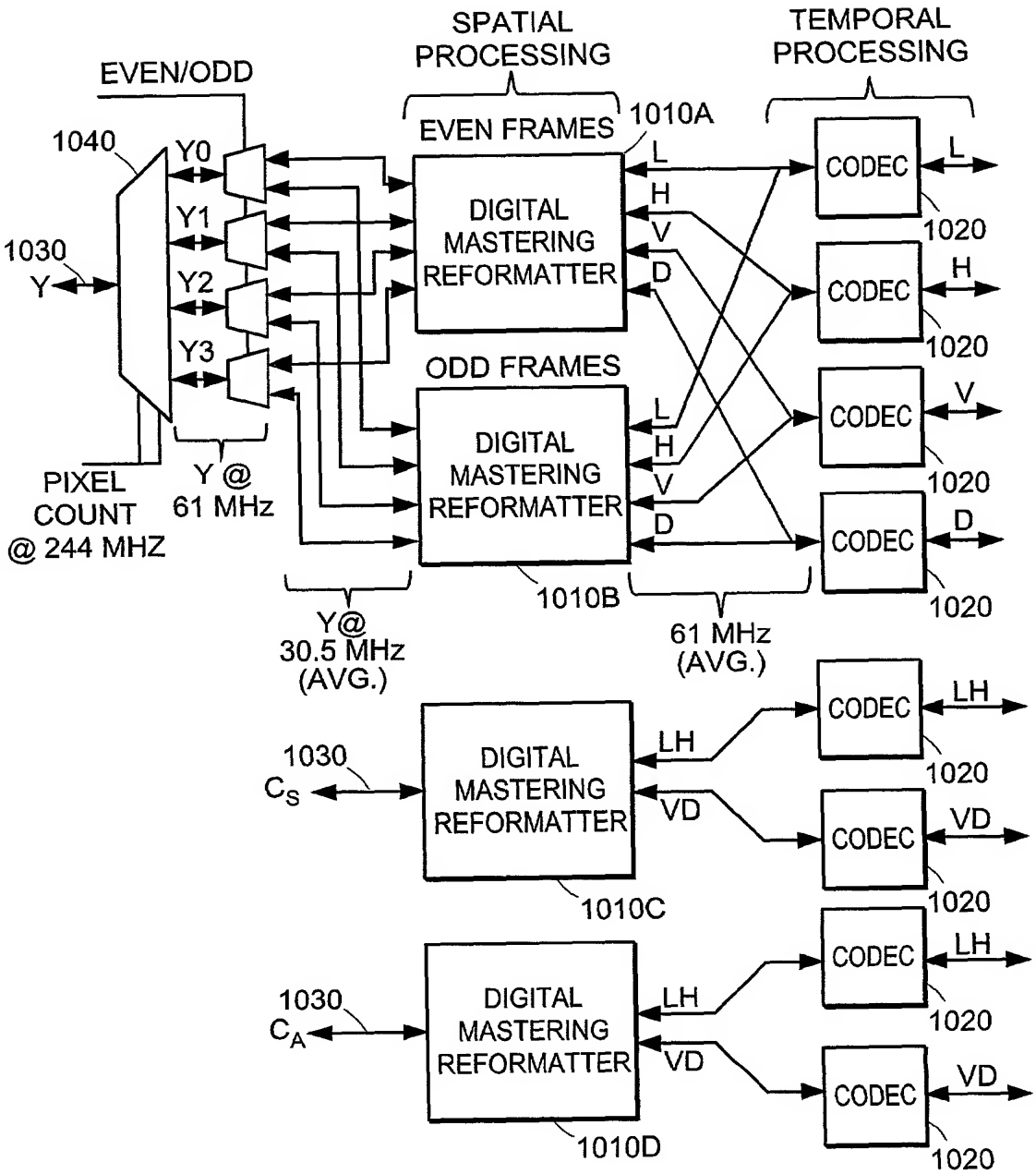
SPATIAL PROCESSING
TEMPORAL PROCESSING
EVEN/ODD
1040
Y0
Y1
Y2
Y3
1030
Y
PIXEL COUNT @ 244 MHZ
Y @ 61 MHz
EVEN FRAMES
1010A
DIGITAL MASTERING REFORMATTER
L
H
V
D
ODD FRAMES
DIGITAL MASTERING REFORMATTER
1010B
CODEC
1020
Y@ 30.5 MHz (AVG.)
61 MHz (AVG.)
1030
C_S
DIGITAL MASTERING REFORMATTER
LH
VD
1010C
1030
C_A
DIGITAL MASTERING REFORMATTER
1010D

FIG. 10